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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/696,393	10/25/2000	Tohru Watanabe	10449-022001	4117

26161 7590 01/13/2005

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EXAMINER	
YE, LIN	

ART UNIT	PAPER NUMBER
2615	

DATE MAILED: 01/13/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/696,393	WATANABE, TOHRU	
	Examiner	Art Unit	
	Lin Ye	2615	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 August 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,6-12,15 and 16* is/are rejected.

7)☒ Claim(s) *2-5,13,14,17 and 18* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *27 February 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments filed 8/27/04 have been fully considered but they are not persuasive as to claims 1, 6-12, 15 and 16.

For claims 1, 12 and 16, the applicant argues that the Watanabe reference does not teach or suggest an image signal processor for processing a plurality of image signals associated with each of a plurality of screens for determining the real deficient pixels. The examiner disagrees. The Watanabe reference discloses an image signal processor that goes through the candidate (target) pixel registration mode, accumulated value calculating mode and defective pixel determining mode for determining the real deficient pixels and correcting the signal of the deficient pixels. The **accumulated value**-calculating mode is associated with a plurality of screens (e.g., a plurality of photo-electrically converted outputs as a plurality of screens for all the target pixels, such as 1/30sec per frame, see Col. 7, lines 34-35; each of new screens image data corresponding to the all the target pixels are added, the accumulated value calculating operation is repeated N-1 times, see Col. 10, lines 10-30). The defective pixel determining mode is based on the **accumulated value** and second threshold value to determine the actually defective pixels (See Col. 10, lines 57-65). This can be considered as the defective pixel determining mode that detects the defective pixels over the plurality of screens.

In applicant's specification page 9, lines 1-25, describes " the deficiency determining circuit (14) determines whether a pixel corresponding to the address stored in the position

memory circuit 13 is a real deficient pixel or not, based on the continuity of a deficiency candidate (target pixel) over a plurality of **screens**... therefore, the deficiency determining circuit 14 determines a real deficient pixel...". The plurality of screens actually is the plurality of outputs corresponding to the target pixel over a predetermined time period.

The applicant should be noted that the Watanabe reference also discloses a method from the prior art that comparing each of outputs of the target pixel with a threshold value over a plurality of screens (e.g., ten screens) (See Col.2, lines 1-10). It is well known to one of ordinary skill in the art at the time to see more advantages for a method of detecting a deficient pixel in a plurality of pixels associated with each of a plurality of screens so that erroneous detection because of noise or the like can be prevented.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> ((e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 1, 7-8, 12 and 15-16 are rejected under 35 U.S.C. 102(e) as being anticipated by Watamabe et al. U.S. Patent 6,002,433.

Referring to claim 1, the Watamabe reference discloses in Figure 1, an image signal processor (100) for processing a plurality of image signals associated with each of a plurality

of screens (e.g., a plurality of photo-electrically converted outputs as a plurality of screens for all the target pixels, such as 1/30sec per frame, see Col. 7, lines 34-35; each of new screens image data corresponding to the all the target pixels are added, the accumulated value calculating operation is repeated N-1 times, see Col. 10, lines 10-30), comprising: an image memory circuit (4) for storing a signal corresponding to a target (to be possible defective) pixel and signals corresponding to a plurality of peripheral pixels adjacent to the target pixel (all pixels) as shown in Figure 2 (See col. 5, lines 60-67); a deficiency candidate detection (candidate pixel registration mode, see Col. 6, lines 45-65) circuit (11), connected to the image memory circuit, for comparing (comparator 11) the signal of the target (candidate) pixel with a threshold value (THL1) set in accordance with the signals of the plurality of peripheral pixels (shown in Figure 7) to detect a deficient pixel candidate; a deficiency determining (defective pixel determining mode, see Col. 7, lines 57-67) circuit (15), connected to the deficiency candidate detection circuit, for determining a deficient pixel according to continuity of the deficient pixel candidate, detected by the deficiency candidate detection circuit (stored in candidate pixel memory 8), over a plurality of screens (e.g., the defective pixel determining mode is based on the **accumulated value** and second threshold value to determine the actually defective pixels, see Col. 10, lines 57-65; this can be considered as the defective pixel determining mode that detects the defective pixels over the plurality of screens); a position memory circuit (defective pixel memory 16), connected to the deficiency determining circuit, for storing deficiency information of a position of the deficient pixel determined by the deficiency determining circuit; and a deficiency correction circuit (interpolation circuit 40 as shown in Figure 5), connected to the position memory

circuit (16), for correcting the signal of the target pixel which is deficient in accordance with the deficiency information (See Col. 13, lines 56-61).

Referring to claim 7, the Watamabe reference discloses wherein the deficiency determining circuit (15) receives image pickup control (mode signal) information from an image pickup device for producing the image signal and determines a deficient pixel by using the image pickup control information and the threshold value (THL2 , See col. 7, lines 11-25).

Referring to claim 8, the Watamabe reference discloses wherein the deficiency determining circuit receives the image pickup control information from the image pickup device, estimates a luminance (the accumulated value from a incident light from the subject forms an image on CCD 2) of a subject from the image pickup control information, and determines a deficient pixel by using the threshold value (THL2) when the estimated luminance of the subject lies within a predetermined range (See Col. 7, lines 15-55).

Referring to claim 12, the Watamabe reference discloses in Figure 1, A method of detecting a deficient pixel in a plurality of pixels associated with each of a plurality of screens (e.g., a plurality of photo-electrically converted outputs as a plurality of screens for all the target pixels, such as 1/30sec per frame, see Col. 7, lines 34-35; each of new screens image data corresponding to the all the target pixels are added, the accumulated value calculating operation is repeated N-1 times, see Col. 10, lines 10-30), comprising the steps of: detecting a deficient pixel candidate by comparing a signal of a target pixel in one of the plurality of screens with a threshold value (THL1) set in accordance with signals of a plurality of peripheral pixels adjacent to the target pixel (candidate pixel registration mode,

see Col. 6, lines 45-65); storing a position of the detected deficient pixel candidate (in position data memory 9 of memory 8); recomparing a signal of that target pixel in another of the plurality of screens which corresponds to the position stored in the position storing, step with the threshold value (THL2, the Watanabe reference also discloses a method from the prior art that comparing each of outputs of the target pixel with a threshold value over a plurality of screens, e.g., ten screen, See Col.2, lines 1-10); storing a comparison result of the recomparing step; repeating the recomparing step and the comparison result storing step a predetermined number of times (N-1 times) over the plurality of screens (e.g., the defective pixel determining mode is based on the **accumulated value** and second threshold value to determine the actually defective pixels, see Col. 10, lines 57-65; this can be considered as the defective pixel determining mode that detects the defective pixels over the plurality of screens); and detecting a deficient pixel in accordance with a plurality of comparison results obtained by the repeating step (defective pixel determining mode, see Col. 7, lines 57-67).

Referring to claim 15, the Watamabe reference discloses wherein the deficient-pixel detecting step detects a deficient pixel in accordance with a plurality of comparison results (comparing with difference threshold TH1 and variable THL2) and an image pickup condition for producing image signals (by an interpolating circuit 40, and see Col. 13, lines 55-61).

Referring to claim 16, the Watamabe reference discloses in Figure 1, a method of detecting a deficient pixel in a plurality of pixels associated with each of a plurality of screens (e.g., a plurality of photo-electrically converted outputs as a plurality of screens for all the target pixels, such as 1/30sec per frame, see Col. 7, lines 34-35; each of new screens

image data corresponding to the all the target pixels are added, the accumulated value calculating operation is repeated N-1 times, see Col. 10, lines 10-30), comprising the steps of: detecting a first deficient pixel candidate by comparing a signal of a target pixel in one of the plurality of screens with a threshold value set in accordance with signals of a plurality of peripheral pixels adjacent to the target pixel (candidate pixel registration mode, see Col. 6, lines 45-65); storing a position of the first deficient pixel candidate (in position data memory 9 of memory 8); detecting a second deficient pixel candidate by comparing a signal of the target pixel in another of the plurality of screens with the threshold value; determining if a position of the first deficient pixel candidate coincides with a position of the second deficient pixel (candidate defective pixel determining mode, see Col. 7, lines 57-67); updating information of the stored position of the first deficient pixel candidate in such a way that only position information of that first deficient pixel candidate which has been determined to have a match in the coincidence determining step remains (stored in defective pixel memory 16); repeating the second-deficient-pixel-candidate detecting step, the coincidence determining step and the updating step by a predetermined number of times (N-1 times) over the plurality of screens (e.g., the defective pixel determining mode is based on the **accumulated value** and second threshold value to determine the actually defective pixels, see Col. 10, lines 57-65; this can be considered as the defective pixel determining mode that detects the defective pixels over the plurality of screens); and detecting a deficient pixel in accordance with position information (position data memory 9) of deficient pixel candidates acquired by the repeating step (Col. 6, lines 31-36).

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Watamabe et al. U.S. Patent 6,002,433.

Referring to claim 1, the Watamabe reference discloses wherein the position memory circuit includes: a first memory (candidate pixel memory 8) for temporarily storing position information of the deficient (candidate for possibly defective) pixel (position data memory 9 inside of memory 8) together with a result (level data memory 10 inside of memory 8) of detection by the deficiency candidate detection circuit (11); and a second memory (defective pixel memory 16) for storing the position information of the deficient (defective) pixel read from the first memory (8) as shown in Figure 1. However, the reference does not explicitly states the second memory (16) is non-volatile memory. Office Notice is taken both the concept and the advantages of providing a non-volatile memory for the defective pixel memory (16) is well know and expected in the art. It would have been obvious to have a non-volatile memory in Watanabe as the memory are known to retain their contents (deficient pixel information) when power is turned off.

6. Claims 9-10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Watamabe et al. U.S. Patent 6,002,433 in view of Suzuki U.S. Patent 5,327,246.

For claims 9-10, the Watamabe reference discloses all subject matter as discussed in respected claim 1, except the reference does not explicitly show the deficiency determining circuit determines a deficient pixel repeatedly in a time division multiplexed manner for each of a plurality of segmental areas of one screen instead of all pixels.

The Suzuki reference discloses in Figures 1 and 7, an image processing circuit including the deficiency determining circuit determines a deficient (defect) pixel repeatedly in a time division multiplexed manner for each of a plurality of segmental areas (a candidate pixel value group output from the candidate pixel value group sampler 3, see Figure 7 and Col. 4, lines 8-20) of one screen. The Suzuki reference is evidence that one of ordinary skill in the art at the time to see more advantages of the image processing apparatus can determine the defect pixel by using a candidate pixel value group with surrounding the target (to be possible defective) pixel instead using all pixels in the image pickup sensor so that the deficient pixel can be more quick and accurate. For that reason, it would have been obvious to the image processing apparatus including the deficiency determining circuit determines a deficient pixel repeatedly in a time division multiplexed manner for each of a plurality of segmental areas of one screen disclosed by Suzuki.

7. Claim 11 is rejected under 35 U.S.C. 103(a) as being unpatentable over Watamabe et al. U.S. Patent 6,002,433 in view of Tan et al. U.S. Patent 6,381,357.

For claim 11, the Watamabe reference discloses all subject matter as discussed in respected claim 1, except the reference does not explicitly show at least one of the deficiency determining circuit and the correction information memory circuit is connected to an external

unit via a bus and a determination condition for a deficient pixel including the threshold value is altered by the external unit.

The Tan reference discloses in Figure 5, a defective pixel detection system having the deficiency determining circuit (processor 512) and the correction information memory circuit (511) is connected to an external unit (monitor 520) via a bus (system bus 513 and i/o bus 515) and a determination condition for a deficient pixel including the threshold value (predetermined threshold T may be chosen depending upon a number of device dependent factors) is altered by the external unit (computer 510) (See Col. 4, lines 20-25). The Tan reference is evidence that one of ordinary skill in the art at the time to see more advantages of the deficiency determining circuit and the correction information memory circuit is connected to an external unit via a bus and a determination condition for a deficient pixel including the threshold value is altered by the external unit so that allowing the camera to capture the next object/Scene quickly without additional delay. For that reason, it would have been obvious to the deficiency determining circuit and the correction information memory circuit is connected to an external unit via a bus, and a determination condition for a deficient pixel including the threshold value is altered by the external unit disclosed by Suzuki.

Allowable Subject Matter

8. Claims 2-5, 13-14 and 17-18 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Referring to claims 2-5, 13-14 and 17-18, the prior art does not teach or fairly suggest the deficiency candidate detection circuit compute a difference between a maximum level and a minimum level of the signals of the plurality of peripheral pixels, producing a first threshold value by adding the difference to an average level of the signals of the plurality of peripheral pixels and producing a second threshold value by subtracting the difference from the average level.

Conclusion

9. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Lin Ye whose telephone number is (703) 305-3250. The examiner can normally be reached on Mon-Fri 8:00AM-5:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Andrew B Christensen can be reached on (703) 308-9644. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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Lin Ye
January 5, 2005